Failure Mechanisms in Integrated Circuits

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INTRODUCTION

The two most important points, in the journey of the failure analyst, are the identification of the failure mode and failure mechanism. The failure mode is the observed electrical or visual symptoms that are anomalous to a component's advertised or implied behavior or appearance. Failure modes can range in extremity from catastrophic to slight degradation, and they are typically categorized as functional, parametric, or visual. Functional failures involve problems with the digital logic and the associated circuitry, which cause the device to behave differently than specified. Parametric failures involve analog outputs which are out of tolerance, e.g. I/O pin leakage and discontinuities. Visual reject failures involve devices which have been mismarked, corrosion occurrences, packaging issues, or other easily found defects.

The failure mechanism is the actual physical defect or condition that causes the failure mode to occur. Failure mechanisms can involve reliability, fabrication, design, test, packaging, and environmental or other use issues. For a given failure mechanism, its occurrence has a heavy dependence on the operational and environmental conditions under which the device has operated. A knowledge of the history of the device is critical to be able to effectively diagnose failures. [1].

Identification of the appropriate failure mechanism is nominally the endpoint of the failure analysis laboratory work. Once the failure mechanism has been identified, one could go further to identify the root cause of the failure. The root cause is the fundamental incident or condition that caused the component to fail and can usually be traced to pushing the limits of current fabrication technology, a machine problem, operator error, or sometimes a combination of all. Once the root cause is identified, actions can then be taken to eliminate future occurrences of such errors.

In this paper, we present an overview of common failure mechanisms illustrated with typical micrographs [2]. The main categories of failure mechanisms are chip related and assembly related failure mechanisms. Chip related failure mechanisms typically involve process issues such as particle defects, contamination, oxide defects, shorted metal, and diffusion or substrate defects. Assembly related failure mechanisms include problems which arise during the packaging of the device after processing. These can include chip and package cracks, protective over-coat (PO) damage, and bonding issues. The advent of the flip chip device technology has also ushered in a new breed of failure mechanisms to the world of failure analysis. Failures involving Flip Chip technology often result from the unique packaging structure of the device itself.

CHIP RELATED FAILURE MECHANISMS

In the section below, a few examples of typical chip related defects are reviewed: Particulates and Contamination, Gate Oxide Defects, Multi Level and Metal Interlayer Oxide Defects, Poly Layer Defects, Metal Layer Defects, Protective Overcoat (PO) Defects, Lithographic Defects, Open Contacts, Shorted Contacts, Laser Repair Defects, Silicide Extrusions, Filaments, and Substrate Defects.

Particle Defects/Contamination

Contamination related failures are typically categorized into three groups: ionic contamination, foreign contamination (particles), and process etch residue.

Ionic Contamination. Ionic contamination is a non-visual defect associated with the presence of ions (such as

hydrogen or sodium) in sensitive areas within the device. Sodium is a common contaminate in the fabrication process due to its presence in the atmosphere, sweat, and breath, in the form of NaCl. Ionic fail mechanisms are typically bake recoverable and are usually seen following burn-in. Clearly, ionic contaminates can alter the electrical properties of the device and, in the case of sodium, will cause significant changes in the threshold voltage (V_t) and junction leakage. These types of defects subside with a high temperature bake with no bias as the mobile ions that collect at the PN junctions and gate oxide disperse.

Foreign Particles. Foreign particles can typically be traced to process equipment and personnel. Fig. 1 shows a DRAM device, which showed a column failure. Using the electrical signature, the failure was traced to gate oxide particles measuring approximately 0.4um, which created a leakage path at the p-channel pull-up transistor of the failing sense amplifier. The fail mechanism of this device was determined to be particulate contamination (possibly residual nitride) before gate oxidation. Similar examples of particulate contamination.are shown in Figures 2 and 3.

Fig. 1. Particulate gate oxide contamination.

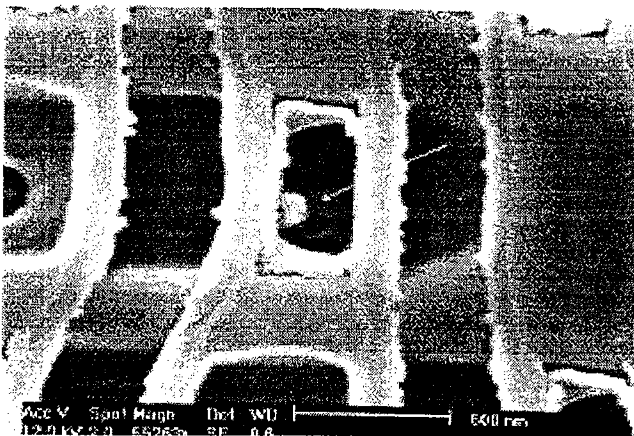

Fig. 2. Storage node contact particle

Fig. 3. Intermetal oxide particle shown after Focused Ion Beam cross sectioning.

Process Etch Residue. Process etch residue is usually associated with particles, but the contamination that blocks the etching process is removed during additional processing. In some cases, however, signs of the residue remain in tact. Fig. 4 shows residue contamination in the form of photoresist. This unit exhibited contamination blocking the guard-ring implantation in the periphery.

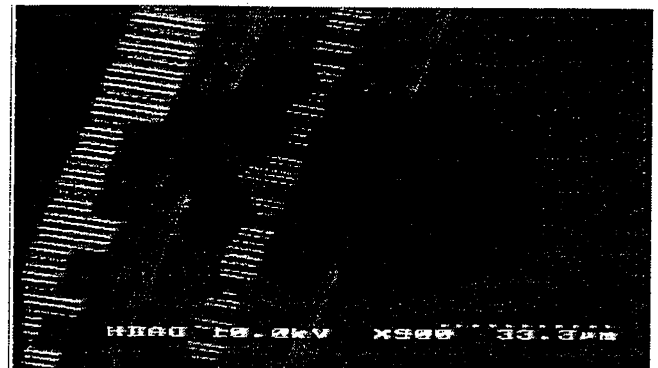

Fig. 4. Photoresist residue contamination.

Gate Oxide Defects

Pinholes. Many common failure mechanisms are related to the integrity of various dielectrics within the device. Defects in gate oxides can cause them to become leaky or shorted when a voltage is applied. Pinholes can be introduced during lithography steps or can arise from particulates into the area. They can also occur due to crystalline defects. With the complexity and size of today's devices, it is becoming evermore challenging to spot these kind of gate shorts visually. Even if a particulate does not produce a discernable hole, it can produce a region which has a lower breakdown strength than the rest of the oxide. Fig. 5 shows a DRAM device exhibiting a single bit logic failure. In this case, the gate oxide pinhole provided a leakage path from the word line to the cell bitline / cell capacitor. The root

cause of the failure was determined to be dielectric failure in the cell transfer gate associated with contamination (most likely residual nitride) before gate oxidation.

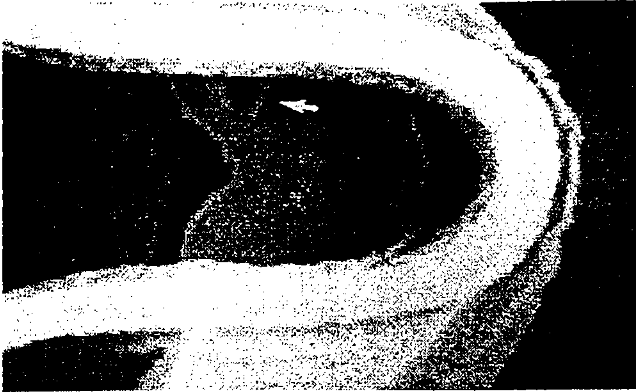

Fig. 5. Gate oxide pinhole pinhole providing a leakage path from the word line to the cell bitline / cell capacitor.

Figures 6 and 7 show other examples of gate oxide pinholes. In Fig. 6, the gate oxide pinhole provides a leakage path from Vpp to the passing word line in the row decoder causing this row to be "stuck on." The root cause was determined to be dielectric breakdown due to gate oxide thinning at the field oxide edge (birds beak).

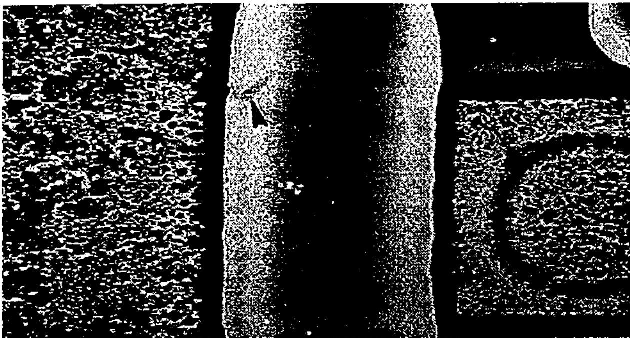

Fig. 6. Gate oxide pinhole providing a leakage path from Vpp to the passing word line in the row decoder.

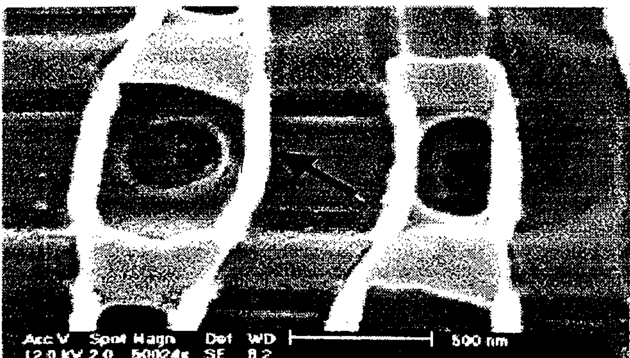

Fig. 7. Gate oxide pinhole in transfer gate.

Breakdown. Oxide pinholes can lead to extreme cases such as gate oxide breakdown. There are two types of breakdown which can exist. The first is due to EOS and ESD while the other is a time dependent breakdown, which can occur during operation within proper conditions. Clearly, EOS and ESD type failures are due to high electric fields which exceed the oxide breakdown field strength. Time dependent oxide breakdown can occur due to a number of reasons, including particulate contamination, ionic contamination, mechanical damage to the oxide, or uneven oxide growth. It has been found that oxide breakdown is not appreciably temperature dependent, but can be accelerated by voltage stressing. Figures 8-11 show examples of gate oxide breakdown.

Fig. 8. Gate oxide breakdown due to EOS/ESD.

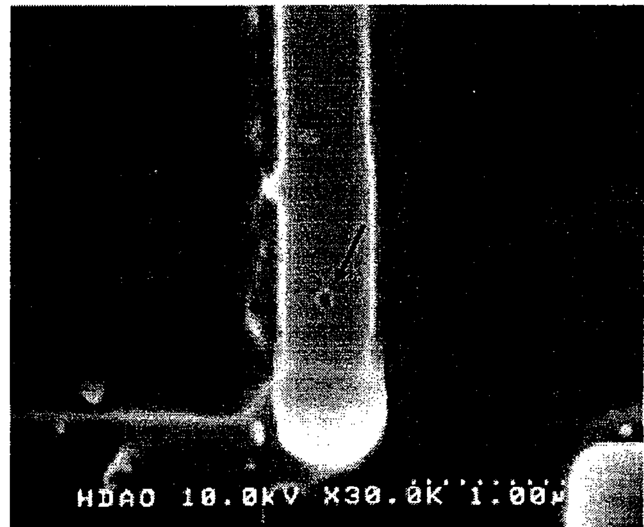

Fig. 9. EPROM device which showed multiple failing rows. After failsite isolation using emission microscopy, the failure was traced to a dielectric breakdown caused by electrical overstress.

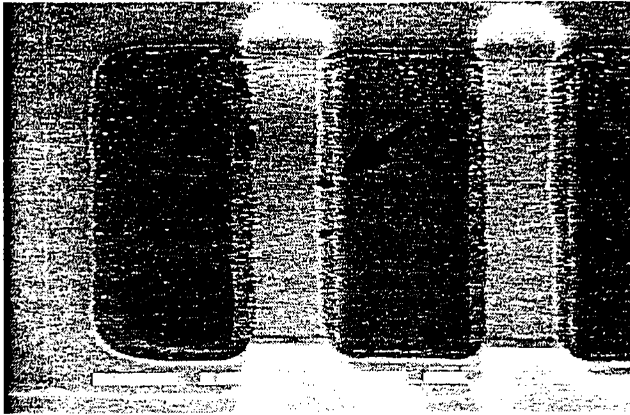

Fig. 10. Gate oxide breakdown caused by EOS/ESD.

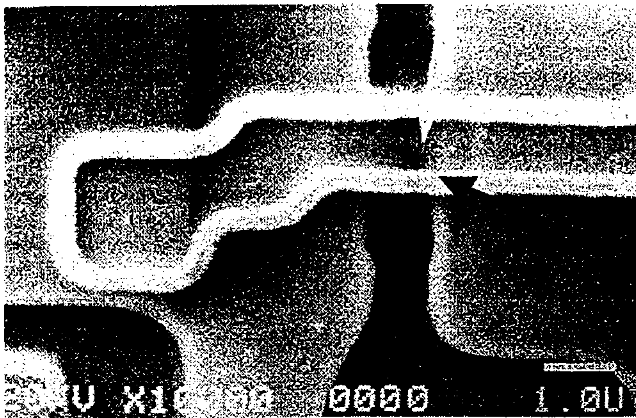

Fig. 11. DRAM cell which exhibited input leakage. After failsite isolation by emission microscopy, the defect was traced to oxide breakdown at the guard ring causing Vcc leakage. The root cause was a dielectric fail caused by the contamination of buried N+ oxide (most likely residual photoresist and nitride) before BN+ oxidation.

Etching Induced Damage. Other oxide related issues can also arise from processing. Fig. 12 shows an etch pit caused during an etching process.

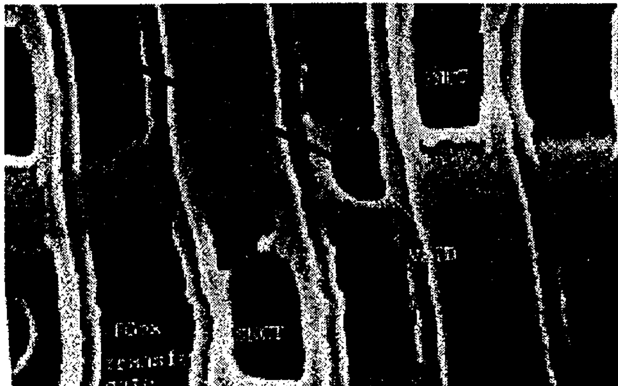

Fig. 12. Field oxide etch pit caused by stacked cell process.

Cracking. In Fig. 13, a DRAM device is shown which failed board level final tests. Failsite isolation by liquid crystal analysis traced the defect to side wall oxide crack which caused low BVDSS (breakdown voltage drain to source) at the field plate diode ESD structure. The root cause was determined to be poor oxide adhesion of side wall as a result of polymer residue left behind after poly gate etch.

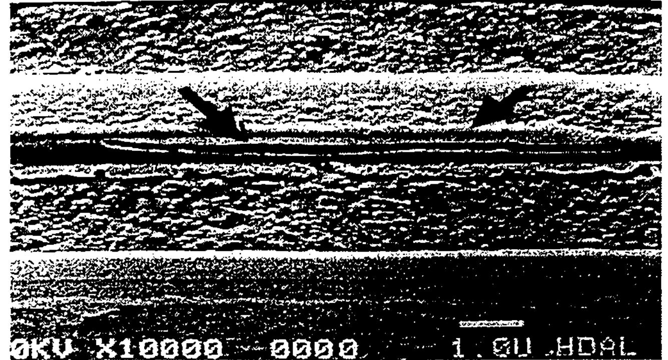

Fig. 13. Side wall oxide crack resulting in low drain to source breakdown voltage.

Multi Level and Metal Interlayer Oxide Defects

Gate oxides are not the only dielectrics which are susceptible to failures. Other oxide layers, such as multi level oxides (MLO) and metal interlayer oxides (MILO) are also candidates for defects.

Cracking. Fig. 14 shows a DRAM device which failed due to Icc power down and block failures. After liquid crystal analysis, the defect was discovered to be an interlayer oxide crack. The failure mechanism for this device was metal two to metal one leakage in the row decoder logic as a result of a metal inter layer oxide crack. The root cause was determined to be an abnormally thin MILO2 layer that was unable to compensate for the high tensile stress of the MILO1 layer.

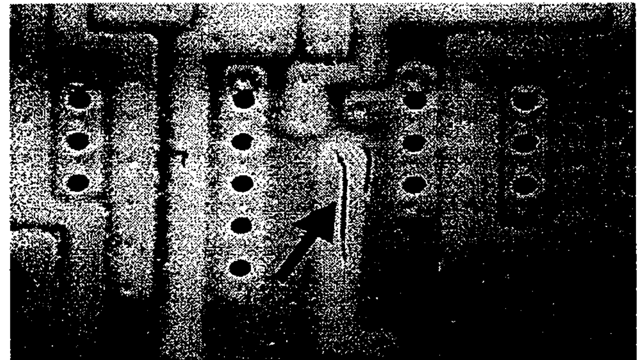

Fig. 14. Metal inter-layer oxide crack causing metal two to metal one leakage.

Delamination. Delamination is also a concern in oxide layers. Fig. 15 shows a DRAM device which exhibited patterned array block failures. Visual analysis revealed that the gross functional failure was due to open metal lines associated with metal inter layer oxide delamination and corrosion. The root cause was determined to be moisture penetration and package stress which resulted in metal inter level oxide delamination. Poor adhesion between metal inter level oxide (MILO) and multi layer oxide (MLO) was also a contributing factor.

Fig. 15. Metal inter layer oxide delamination due to moisture penetration and package stress.

Particulates. Oxide layers are also susceptible to particulate contamination. In Fig. 16, a DRAM device is shown which exhibited shorts. After failsite isolation by liquid crystal analysis, the defect was traced to a particulate contaminate which can be seen at the metal interlayer oxide level after being cross sectioned using a Focused Ion Beam (FIB) workstation. The fail mechanism for this device was a metal interlayer oxide particle measuring approximately 0.5um which provided a leakage path between metal 3 and metal 2 in the device circuitry. The root cause for this mechanism was determined to be dielectric failure caused by particulate contamination prior to metal three lithography. Energy dispersive x-ray (EDX) analysis of the particle revealed calcium, potassium and chlorine.

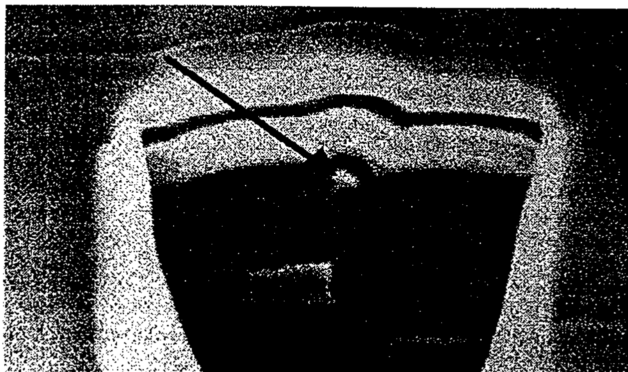

Fig. 16. Particulate contaminate in the metal interlayer oxide.

Poly Layer Defects

Another group of defects are associated with the polysilicon layer. These include mostly particulate contaminates. Figures 17 through 19 show examples of poly layer particulate contamination.

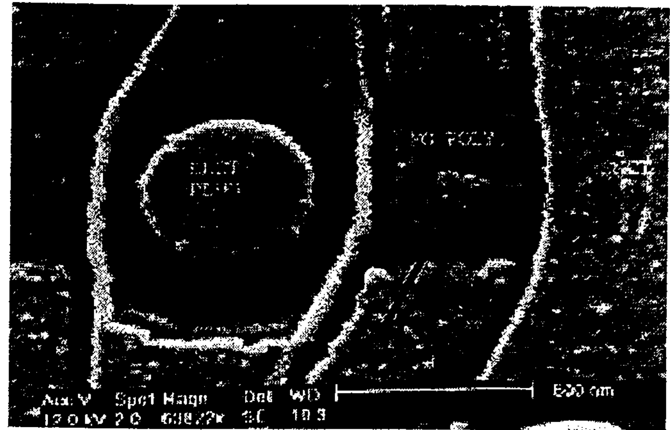

Fig. 17. DRAM device which was deprocessed to poly level using lapping techniques. The arrow indicates a poly particle which should not be there.

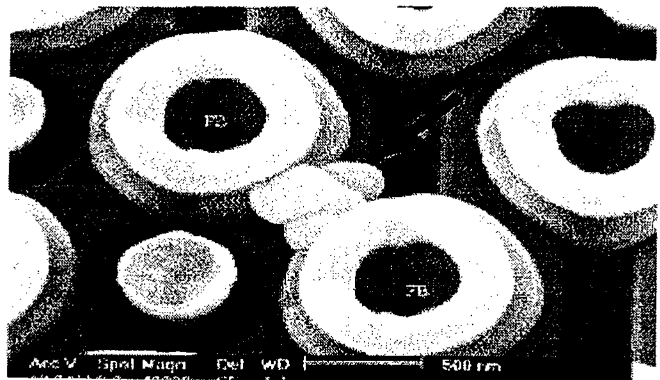

Fig. 18. Contamination of a storage cell (poly two level)

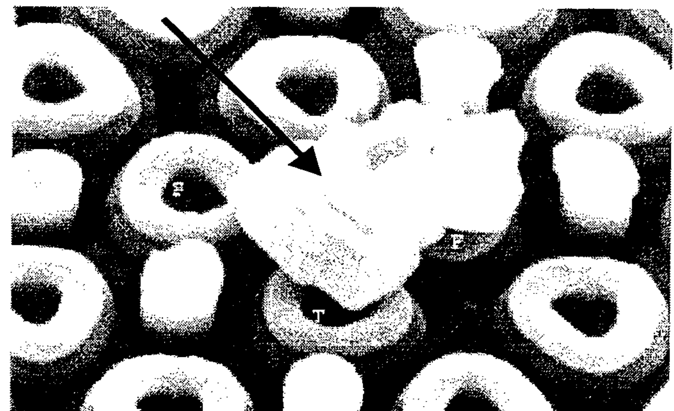

Fig. 19. Particle on top of poly plate

Metal Layer Defects

Typical defects occurring in metal layers are due to particulates and electromigration; however, other cases may be lithography, etch, or stress induced. (The stress can be mechanical, electrical, or thermal.)

Particulates. Figures 20 through 22 show examples of metal layer particulate contamination. Fig. 20 shows an example of metal particulate contamination at the metal one layer. Fig. 21 shows a an FIB cross section illustrating particulate contamination under the metal one layer resulting in degradation of the metal layer. Elemental analysis of the particle revealed the presence of titanium, which caused leakage and subsequent functional failure. Steep dielectric steps create metallization problems such as metal bridging and metal opens. Fig. 22 shows a particulate contamination at the pre- ONO layer.

Fig. 20. Metal particulate contamination at metal one layer.

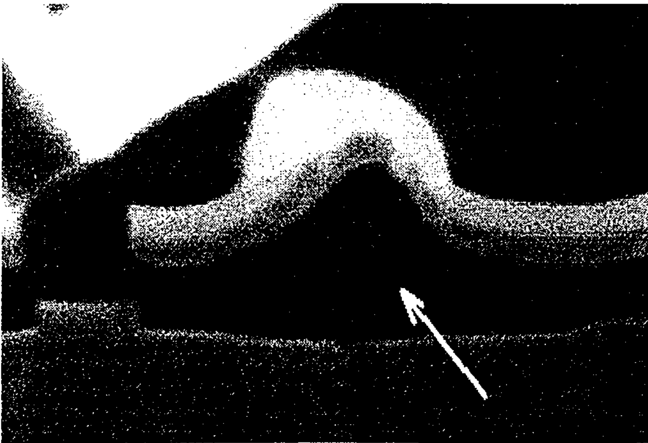

Fig. 21. FIB image revealing metal layer degradation due to particulate contamination.

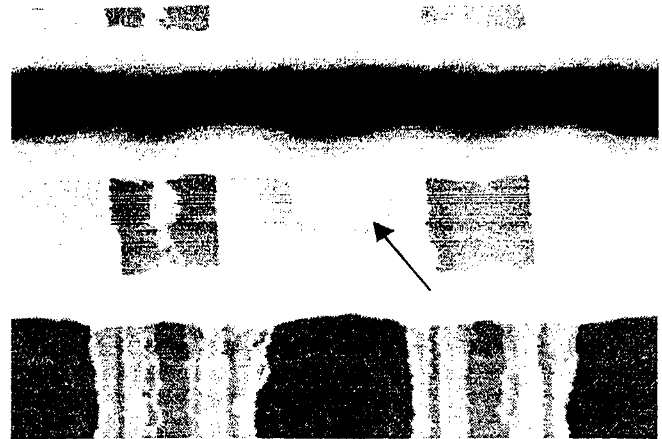

Fig. 22. Metal particulate contamination at pre-ONO layer.

Electromigration. Opens in metal lines due to electromigration occur as thin films are stressed at high current densities. This causes the metal atoms themselves to diffuse in the direction of electron travel and any flux divergence leads to a void or a pileup. Electromigration is a cumulative effect as stresses of short duration will eventually have the effect of a stress of long duration. Fig. 23 shows a DRAM device which failed a field functional array test. Visual analysis revealed an open metal in the clock circuitry as a result of electromigration. The root cause of the failure was determined to be electromigration of the Al:Si metalization due to extended high temperature / high current conditions.

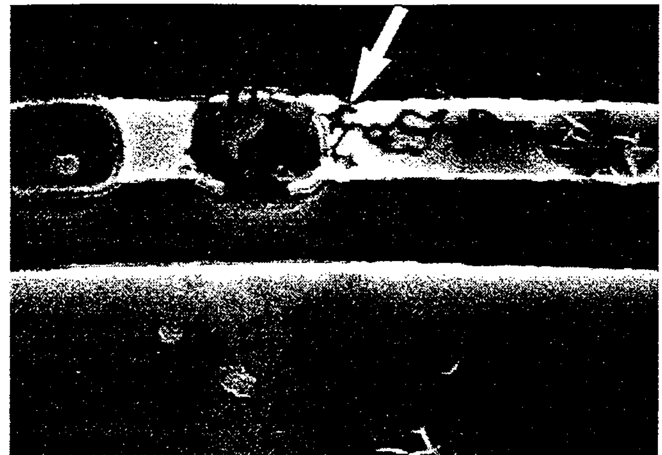

Fig. 23. Open metal due to electromigration

Stress Induced Failures. Fig. 24 shows a DRAM device which exhibited a partial column failure. In this case, the compressive stress of the nitride passivation was determined to be very high. The failure mechanism was an open metal bit line at the failing column due to metal voiding. The root cause was determined to be Al:Si metalization "creep" caused by high compressive stress of the overlying nitride passivation.

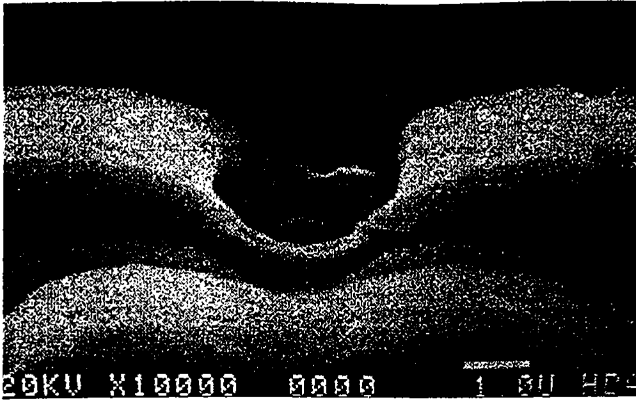

Fig. 24. Open metal at failing bit column due to metal voiding.

Protective Overcoat Related Defects

Breadloafing. PO contamination failures consist of those failures originating from particles or residue. Problems can also arise from PO coverage issues. Fig. 25 shows a poly level defect which was the result of a PO process. The image shows an EPROM device which exhibited a single bit data retention failure. After failsite isolation based on the electrical signature, the device was found to have a crack caused by poor PO coverage ("breadloafing"). The failure mechanism was determined to be a charge loss at the failing cell due to an MLO, poly 2, and ILO crack. The root cause was then determined to be that the MLO most probably originated at the PO layer as a result of PO breadloafing.

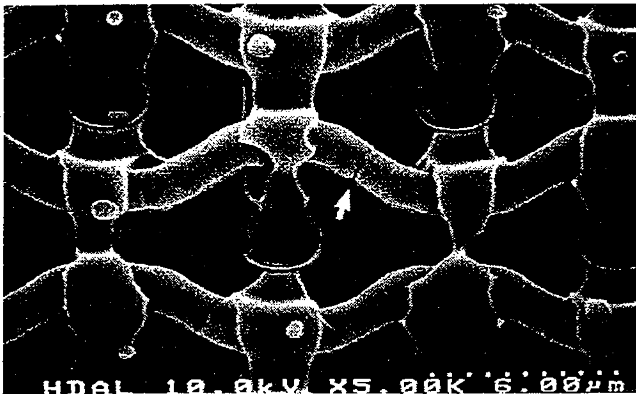

Fig. 25. Results of poor PO coverage seen at poly level.

Lithography Defects

Fig. 26 shows a DRAM device which exhibited moat to moat leakage in the internal logic circuitry Comparison of this unit to a control unit revealed a narrow moat-moat spacing. The control unit had a 1.1 um spacing whereas the failing one had a .50 um spacing. The root cause of this failure was determined to be improper moat sizing during patterning.

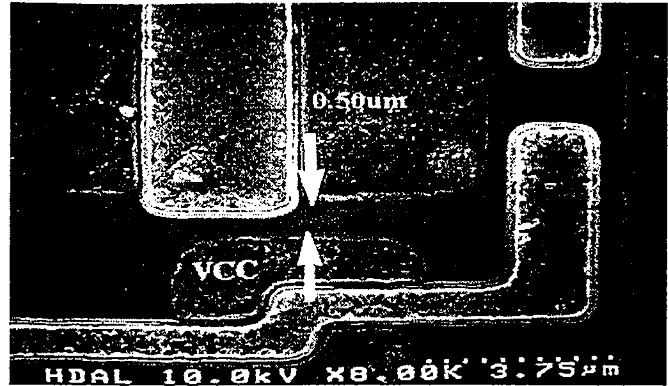

Fig. 26. Moat to moat leakage due to improper moat sizing.

Open Contacts

With the ever increasing aspect ratios required for multi level devices, proper contact formation has become an increasing challenge. Contacts may become open due to reasons ranging from the presence of silicon nodules, residual oxide, contamination, or incomplete etching.

Nodules. Silicon nodules occur when Al:Si metal is deposited into a contact via and is allowed to slowly cool. As the temperature drops, so does the solid solubility of the Si in the Al, and the result is the precipitation of Si onto the outside of the metal. This undoped silicon raises the resistance of the contact substantially. An example of silicon nodule resistance is seen in Figure 27.

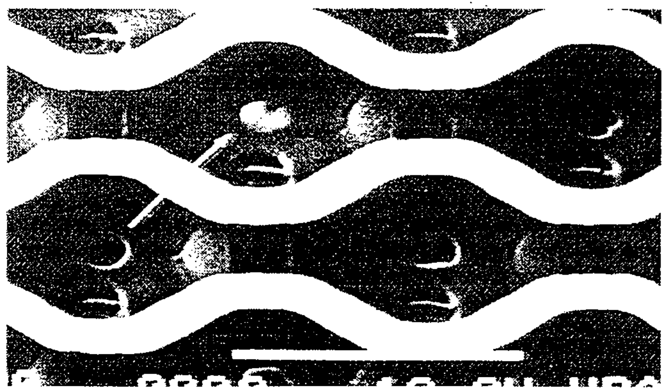

Fig. 27. Silicon nodule causing open/resistive poly plug/metal one contact.

Contamination. Localized particulate contamination can also prevent complete contact etching and the proper filling of the via. Figures 28 and 29 show examples of incomplete metal deposition within the contact via. The root cause of these failures was determined to be incomplete metal step coverage as a result of contamination prior to metal

deposition. Fig. 30 shows an example of incomplete etching during contact formation. In this case, the two step contact etch process only succeeded in performing one step at the failing contact. The root cause was most likely contamination related.

Fig. 28. Open / resistive bit line contact due to particulate contamination.

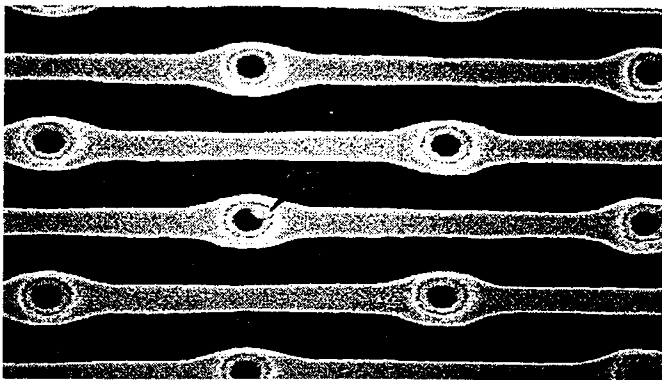

Fig. 29. Open/resistive bit line contact common to the failing bits as a result of particulate contamination.

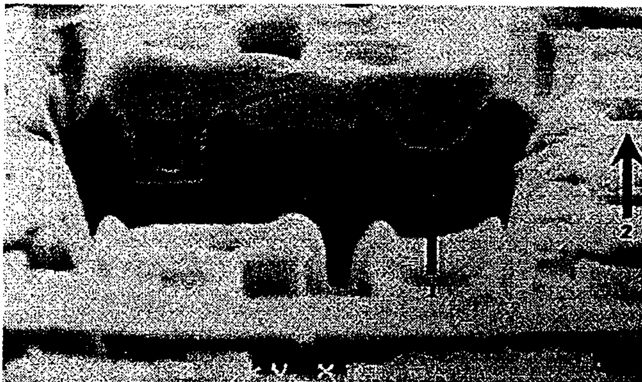

Fig. 30. FIB cross section of an SRAM device which revealed an incomplete oxide etch leading to an open metal to the moat contact at the failing RAM cell.

Stress Induced Failures. In many cases, a void in a metal trace can occur due to stress from an overlying passivation layer. This stress may be thermal mechanical, caused by the differing coefficients of expansions of the metal and the passivation. The compressive stress of the passivation can also be a factor. Fig. 31 shows a EPROM device which underwent failsite isolation by voltage contrast. It was determined that the row address line was disconnected from the nand gate control circuitry in row decoder as a result of open metal to poly contact. The root cause of the failure was determined to be an open contact caused by Al:Si voiding resulting from excessive compressive stress of the oxynitride passivation.

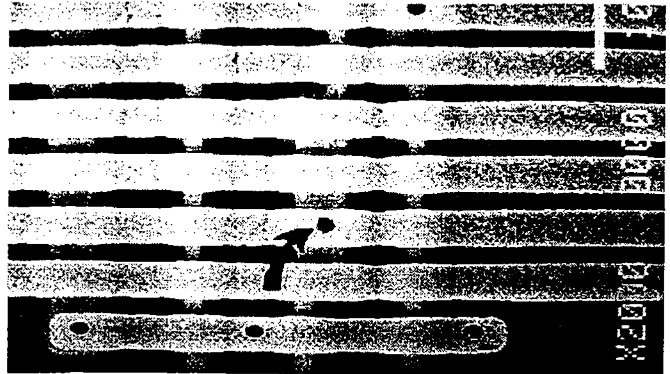

Fig. 31. Open contact due to compressive stress of overlying passivation.

Shorted Contacts

Shorted contacts are usually associated with electrical overstess (EOS) or electrostatic discharge damage (ESD). The example shown in Fig. 32 shows a blown contact due to spiking. Contact spiking can occur in Al:Si metal systems when the silicon content is low or when the sintering temperature is too high. Contact spikes can also occur during deprocessing if hot chucks are used above 450 degrees Celsius. Spiked contacts are similar to blown contacts but generally are characterized by tiny pits in the contact.

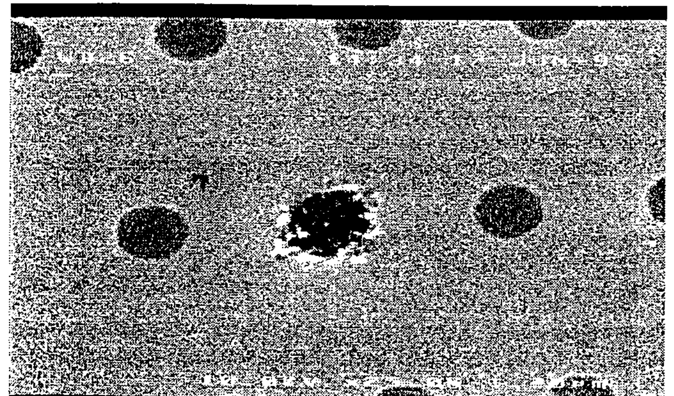

Fig. 32. Blown contact due to spiking.

Laser Repair Defects

Laser repair defects have become more common as more devices use redundancy in memory arrays. The laser fuses are usually polysilicon lines that are fused open with a pulse to set a specific memory address to be replaced by a redundant address. Fig. 33 shows a DRAM device which showed logic failures on half a row. After visual analysis, the defect was found to be a rresistive poly word line adjacent to laser repaired rows due to misaligned and over-powered laser repair.

Fig. 33. Misaligned and overpowered laser repair.

Silicide Extrusions

Silicided polysilicon lines have become popular in reducing the poly interconnect resistance. One problem associated with this technology involves titanium silicide ($TiSi_2$) and BPSG MLO. Fig. 34 shows a silicide extrusion was formed during the BPSG high temperature reflow and densification process. Although the defect appears to be silicide related, the root cause was primarily the MLO processing.

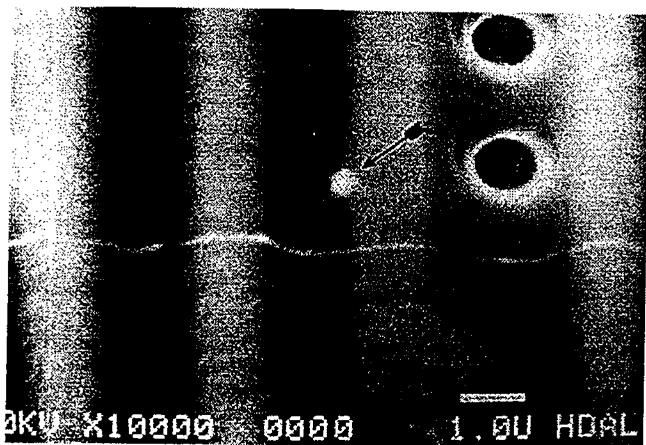

Fig. 34. Titanium silicide extruding from multilevel oxide layer, causing a short from the poly layer to the above metal line.

Filaments

Filament defects typically occur due to the incomplete etching of a metal layer which results in an inadvertent bridge between two conductors. Occurrences of filaments can also be caused by etch residue. The term has also come to include occurrences of poly melt filaments caused by EOS/ESD damage. Figures 35 through 37 show examples of metal and poly filaments.

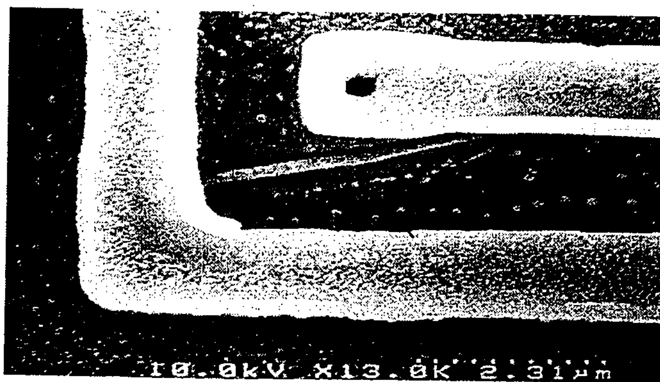

Fig. 35. Metal Filament which has broken off of the bottom metal line to short the two lines together.

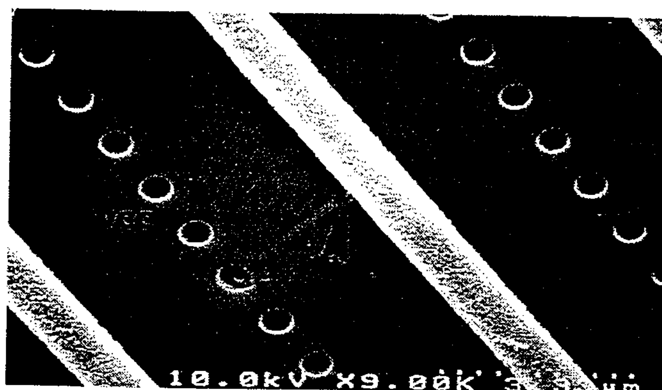

Fig. 36. Poly melt Filament resulting in a short.

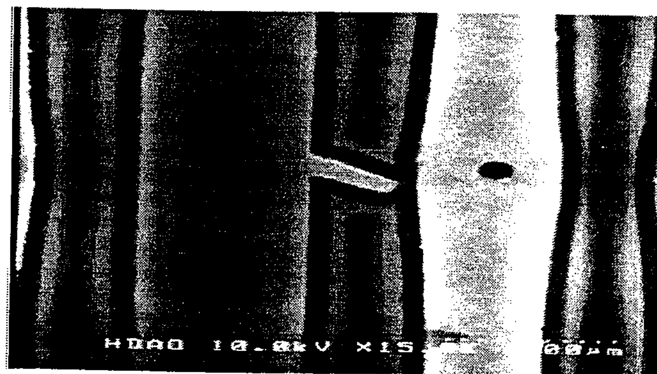

Fig. 37. Metal patterning defect causing a leakage/short to the adjacent failing column.

Substrate Defects

Substrate defects can be caused by oxygen precipitation during crystal growth, metal impurities in the silicon, or implant damage or stress induced during wafer processing. A dislocation can be present in the substrate without causing a failure. The dislocation must be electrically active to induce a failure. Most of the silicon dislocations which occur naturally are rendered inactive by H_2 sintering.

The example in Fig. 38 shows implant related dislocations at the gate region of P-channel transistors. Fig. 39 is a transmission electron microscope (TEM) cross section of a the failure, showing a loop dislocation in the silicon from source to drain under the channel region.

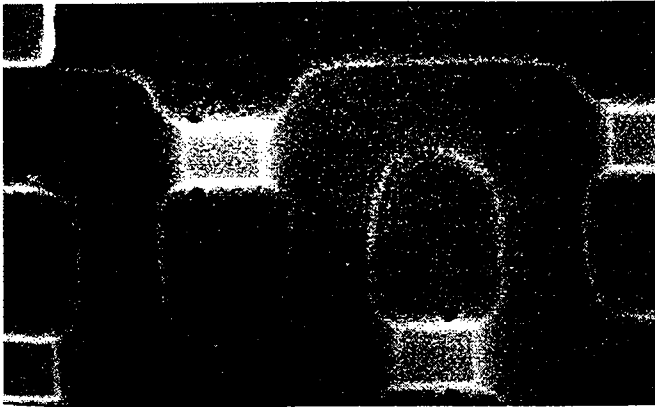

Fig. 38. Silicon dislocation.

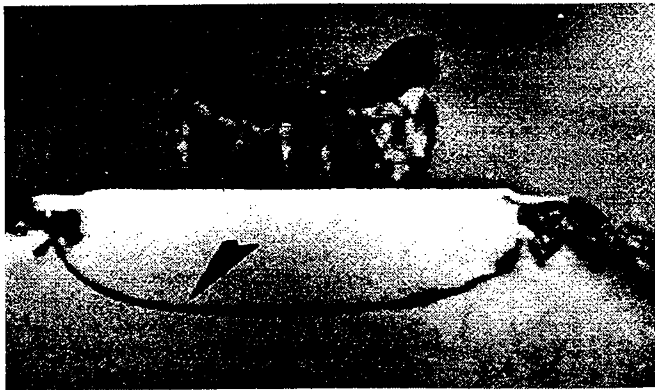

Fig. 39. TEM cross section of Fig. 38.

ASSEMBLY RELATED FAILURE MECHANISMS

The major steps in IC assembly are wafer backgrind, saw, chip mount, wire bonding, molding, lead finishing, trim and form, and symbolization. The typical overall yield is in the upper 90's. Despite this high yield, the assembly process can still have many failure mechanisms under accelerated reliability testing. The accelerated testing is done by the application of high temperature, high humidity, high voltage, or a combination of these. In some cases, mechanical or themo-mechanical stresses are applied to screen for any structural flaws or design weaknesses. Typical failures are bond wire continuity, package cracks, chip cracks, corrosion, passivation cracks, interface delamination, leakage, and parametric failures.

The electrical signature of bond-related failures is typically continuity problems, opens followed by shorts or leakage. Some of the devices will show "input hi" or "input lo" level failures. Generally, these can be detectable if x-ray analysis is done to check for wire or bond related issues. In the case of intermittent contact, performing continuous testing with temperature ramps will typically bring out the failure. Bond strength problems due to low and high bond strengths are detectable by x-ray analysis when the x-ray is taken with a side view shot. They are indicators of potential yield and reliability problems.

Bond wire failures. Figure 40 gives a pictorial view of the failure mechanisms that are associated with the bonding process. Several possible failures can be observed in the diagram. First of all, one must consider the formation of intermetallics at the Al pad/Au wire interface. Some amount of alloying is necessary at this interface to form a good contact, but excessive alloying may cause bond failure. Kirkendall voiding may also be present, where voids within the metals have migrated until merging together at the bond interface [1].

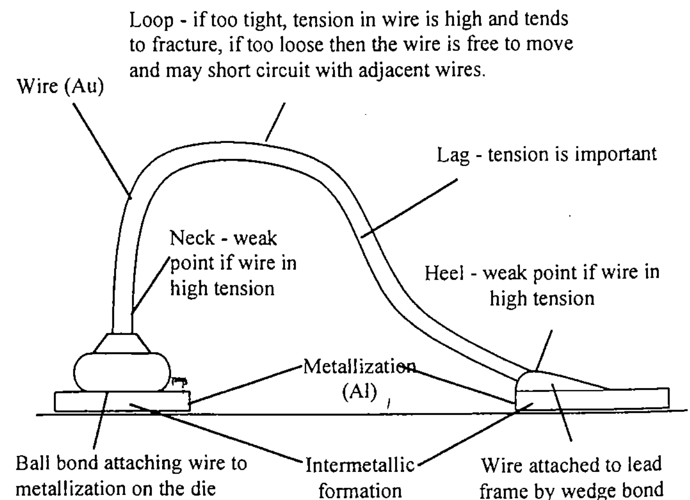

Fig. 40. Reliability issues concerning bonding process [1].

Another parameter in the bonding process which may cause failure is the tension in the bond wire. If the tension is too low, the wire is said to have excessive lag and is susceptible to shorts with other bond wires. An example of

this can be seen in Fig. 41, which shows an example of pin to pin leakage bond wires shorted to adjacent lead frame post. The root cause of this failure was determined to be a bonding machine tension feed failure. If the tension is too high, then the stress at the interfaces can lead to fracturing and opens. Examples of this can be seen in Figures 42 and 43.

Fig. 41. Bond wires shorted to adjacent lead frame.

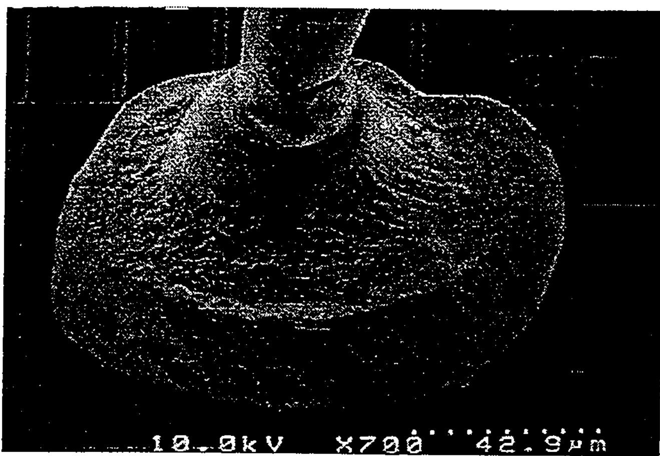

Fig. 42. Cracking at ball bond neck.

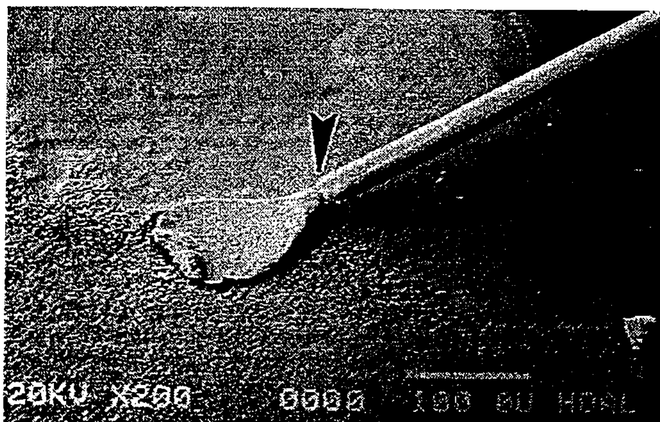

Fig. 43. Cracking at stitch bond.

There are other concerns with the bonding process as well. Moisture has been found to aggravate the metal migration process by the influence of electrolysis. Contamination by impurities such as carbon at the base of the bond can also cause voiding and lead to ball bond lifting. Contamination from chlorine and other impurities can lead to corrosion, as seen in Fig. 44. In this case, corrosion has caused a discontinuity in the bond pad aluminum. EDX analysis detected chlorine at the bond pad. Thus, the root cause of the failure was determined to be corrosion caused by moisture ingress and chlorine contamination.

Fig. 44. Corrosion of bond pad due to chlorine presence.

Fractures within the bond wire itself can also occur. Fig. 45 shows a fractured bond wire at Vcc associated with thermally degraded mold compound. This failure was most likely caused by electrical overstress.

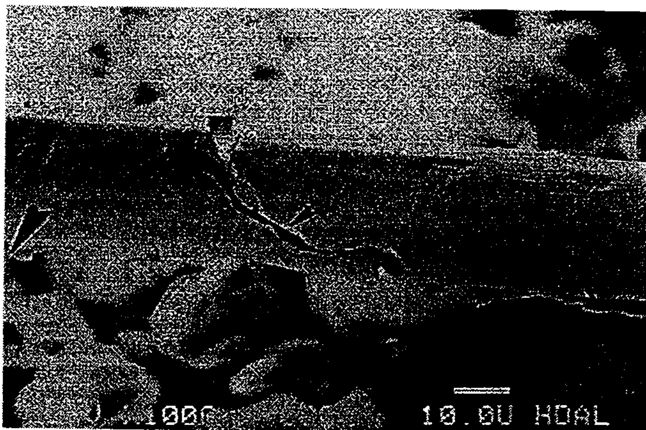

Fig. 45. Fractured bond wire due to EOS

Die Cracks. Fractures in silicon usually originate from the site of the flaw. This flaw can come from a backgrind operation, which leaves behind deep grooves. A high Rt, the maximum surface roughness, is usually indicative of this type of failure. Fractures can also result from saw operations, in which case, the crack origin can be traced to damage on the side of the chip. Other cracks may result from poker pin

damage. In this case, one of the cracks should intersect the poker pin mark, which should be located near the center of the die. Fig. 46 shows a die exhibiting ICC leakage due to a die crack. The root cause of the failure was determined to be a cracked die caused by the lifter pin during the die mount process. Fig. 47 gives an overview of chip and package crack issues.

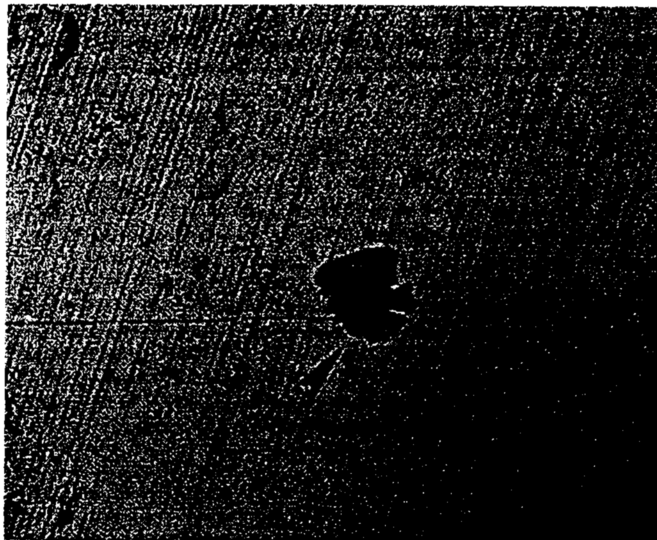

Fig. 46. Cracked die due to lifter pin damage.

Chip and Package Crack Issues	Causes	Distinguishing Feature
Cracked die and Package Cracks	Backgrind damage Saw Wafer mount poker pin Trim and form	Rough backside, High Rt Incomplete cut, Chip Pin mark, Crack thru mark Scuff marks, Imprint Delamination and Internal package crack
	Test handling	Scuff marks
	Surface mount	Package cracks at die edge
	Mold voids	Crack passes through void
	Molding and mold voids	Distortion of mount pad
	Mount epoxy voids	Epoxy viods
	Mount epoxy coverage	Imcomplete coverage
	Design/lay out weakness	PO at scribe
	Interaction with saw	Metal at scribe

Fig. 47. Chip and Package crack issues: their causes and their distinguishing physical features.

Filler Induced PO Damage

The electrical signature of failures due to PO damage for localized point defects in memory devices ranges from single bit cell failures to row and column failures. Recovery of the imprint of the mold is key if identification of filler as the cause is required. Locating PO defects can be done by the use of a metal etch or a Na ion drop test. Partial etching of the PO followed by inspection will also reveal crack patterns that are not obvious, or regions of stress through the crack patterns. X-sections using metallographic techniques can be used to examine PO profiles.

Fig. 48 shows an example of mold compound filler induced PO damage. Analysis involving a mechanical decapsulation confirmed a protruding filler particle. Thus, the root cause was determined to be mold compound filler induced PO damage. Fig. 49 highlights some of the key failure mechanisms related to PO damage.

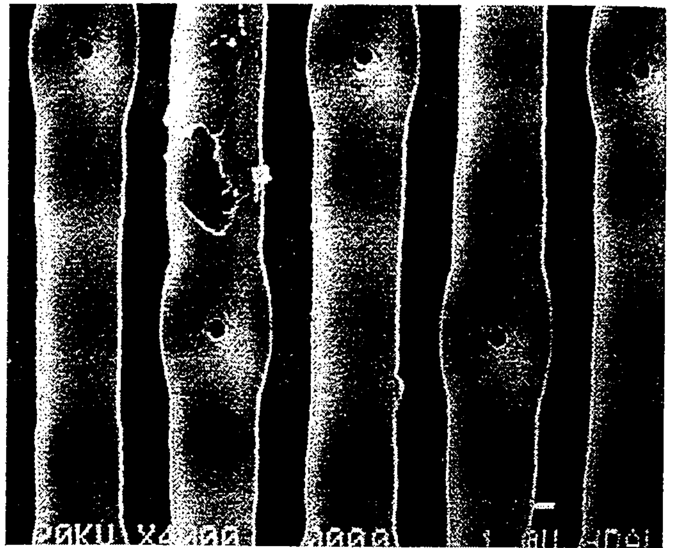

Fig. 48. Mold compound filler induced PO damage.

PO damage issues	Causes	Distinguishing feature
Localized PO defect	Mold compound filler and resin	Compressive fracture cracking at brittle levels
Linear fragment	Design/layout	Metal over poly, long metal runs
Linear scratch	Mold	Scratch lines along mold flow
Point defect	Bond wire	Touches PO during bond
Corrosion	PO stress/voids	X-section xtics, Sharp geometries, corners

Fig. 49. PO damage issues: their causes and their distinguishing physical features.

FLIP CHIP DEFECTS

One of the greatest concerns of the failure analyst at present is the ability to diagnose failures associated with flip chip style devices related to packaging. These failures may include solder bump defects or interfacial abnormalities between the solder bump/substrate and solder bump/die interfaces. An examination of the intermetallic composition of the metallurgy within the bump itself may be necessary to determine the failure mechanisms of some open bumps.

Proper package related fail mechanism identification for flip chip devices typically involves a die pull, die sheer or a traditional cross sectioning of the interfaces within the device. One of the more compelling reasons for performing the cross section is the ability to examine the metallurgical surfaces within the bump. Of particular interest is the consistency of the Sn:Pb bump metallurgy, including the Pb grain size within the bump. Fig. 50 shows an SEM cross sectional image of a bump failing continuity testing. From the cross section, two major anomalies were noted. The first anomaly was the void and possible interface dewetting between the bump and the die interface. The second anomaly was a large Pb band shown at the bottom of the bump in Fig. 50. The Pb band has a tendency to be located near the via, which is the path of the current flow. Due to large amounts of current flowing through the via, the location near it tends to be heated the most, leading to large Pb grain formation at this location. Subsequent curve trace analysis of the bump to the die revealed lack of continuity between the bump and the die, which corroborated our observations.

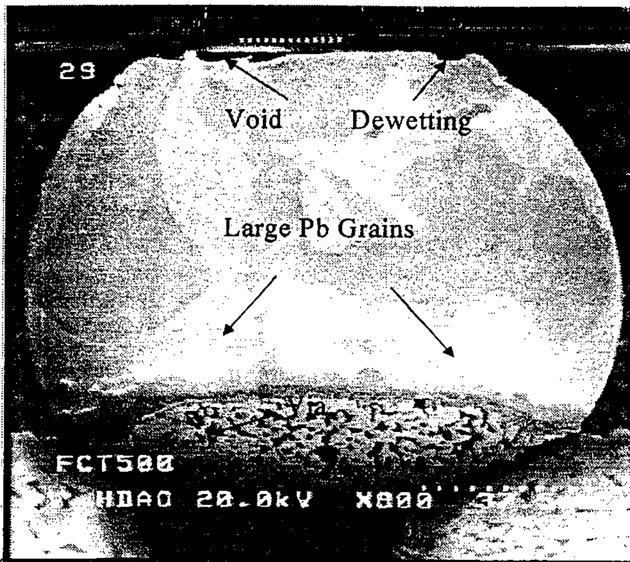

Fig. 50. SEM cross section image of a open bump which separated due to thermal and electromigration effects.

The bump structure shown in Fig. 50 uses a thin layer of Ni/V to separate the Sn of the eutectic (Sn:Pb, 63:37) solder bump from the Al of the top level metal of the CMOS device. If the Sn diffuses through the Ni and reaches the Al interface the bond will be broken. It has been found that this diffusion process is aggravated by the influence of high temperature and hence, the amount of diffusion is a good indicator of the age of the device.. The grain size of the Pb grains within the solder bumps are also good indicators of device age. Fig. 51 shows a cross section of a bump which has undergone tests involving high temperature conditions. The relatively large Pb grain sizes are noteworthy in this case.

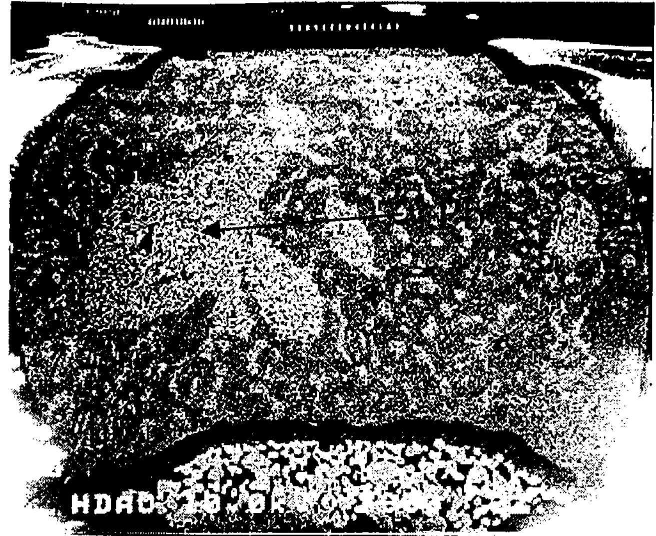

Fig. 51. Cross-sectional SEM micrograph of a bump after high temperature assembly, showing Sn and Pb grain sizes.

Fig. 52 shows the intermetallic formation of the bump shown in Fig. 51. The intermetallic formation is smooth and well defined indicating the diffusion of Sn into Ni.

Fig. 52. SEM micrograph showing the intermetallic formation after high temperature assembly.

The extent of diffusion can also be determined by an EDX analysis of the bump , which reveals the amount of various elements at any point. Fig. 53 is an EDX linescan of the intermetallic formation seen in Fig. 52. As can be seen with respect to the reference line drawn across the linescans, Sn has already started to diffuse into the Ni during the assembly process. Any further heating of the bump will eventually cause failure.

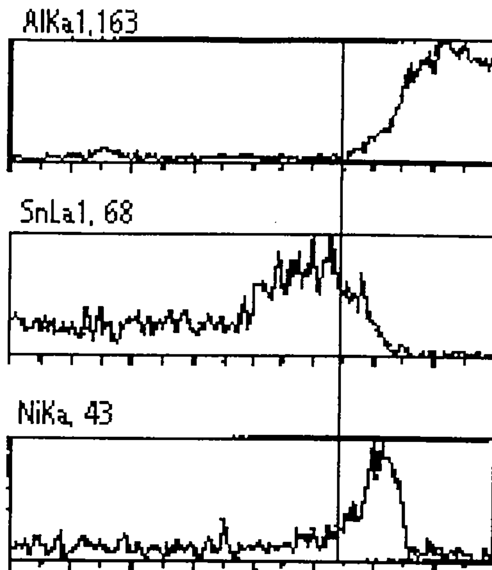

Fig. 53. EDX analysis showing the diffusion of Sn into the Ni, as indicated by the overlap of the elemental graphs

A complementary technique to cross sectioning is the die pull. In this case, the planes of the bump bond can be analyzed visually and by elemental analysis. When the surface of the bump from a die pull is spotted in texture this is an indication Sn has diffused through the Ni causing the bump to de-bond from the Al bond pad. The surface looks spotted in an SEM view as can be seen in Fig. 54.

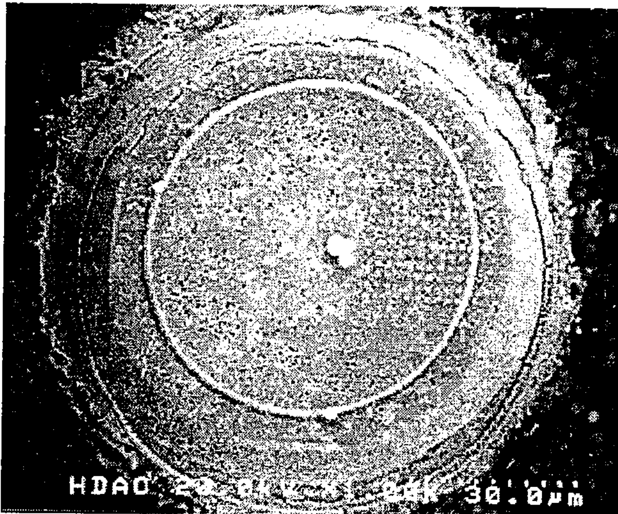

Fig. 54. SEM micrograph of a resistive bump. The bump de-bonded from the Al bond pad.

Fig. 55 shows a failure occuring due to the separation of the solder bump to metal five interface. The failure mechanism determined to be the diffusion of nickel into the Sn:Pb solder causing de-bonding of the Under Bump Metal to metal five of the device.

Fig. 55. De-bonding of bump from metal five interface.

Another solder bump design containing a copper stud within the solder ball is shown in Fig. 56. After high temperature tests, it can be seen that the Pb grain sizes are very large, however, this is not a problem due to the influence of the Cu stud. As the temperature increases, Cu diffusion into the solder bump helps to stabilize the bump. The near infinite source of Cu in the stud prevents the Sn from making contact with the Al of the metal five in the die. The Cu stud does present a reliability issue as bump sizes reduce. Cu is rigid in comparison to the more malleable Sn:Pb solder. In smaller bumps, the Cu takes up a larger percentage of the height. The reduction in the amount of solder in the bump reduces the flexibility giving rise to stress related failures which will be noted later.

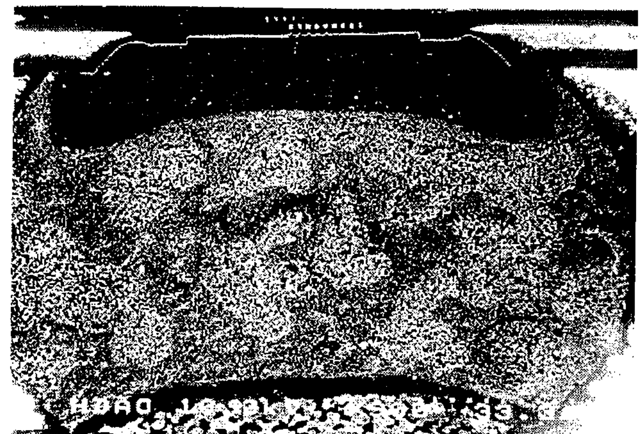

Fig. 56. SEM micrograph of a cross-sectional view of a bump after high temperature testing, showing the Sn and Pb grain sizes. Image used as reference to show alternate bump structure. No failure observed.

In Fig. 57 the result of a die pull of a bump subjected to high temperature operational life (HTOL) testing is presented. Inspection of the bumps after die pull indicated bump melting. The large region of Pb seen in the lower portion of the bump could have this appearance due to voiding in the bump as well as bump melting. However, the crystalline structure of the periphery of the bump (seen in the lower left corner of the image) is indicative of bump melting, which can only occur at temperatures exceeding 183C.

Fig. 57. SEM photograph of a failing bump, which was most likely melted during HTOL testing.

Fig. 58. Bump exhibiting signs of solder fatigue.

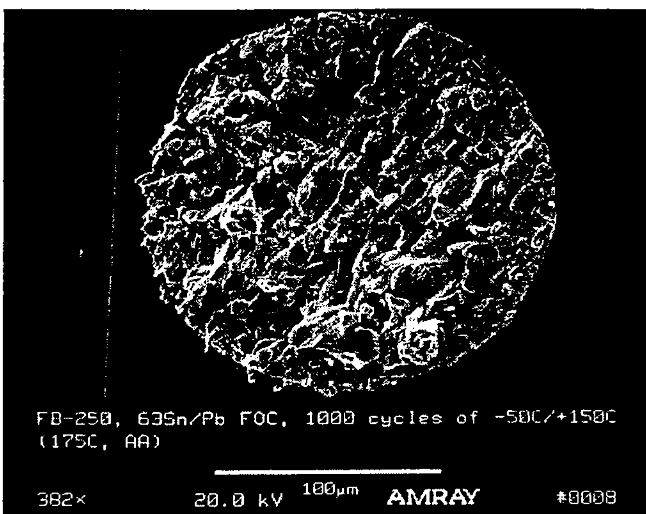

Fig. 59. Cross sectional view of bump in previous image.

There are a plethora of failure mechanisms associated with flip chip packages. Here, we will not discuss all the mechanisms in detail. However, as additional examples, we present Figures 58 through 66 to illustrate several other common failure mechanisms associated with flip chips. Figures 58 through 60 show examples of solder fatigue and creep. Fig. 61 shows a lack of supportive Ti:W layer which has allowed the "rocking" of the solder ball and the subsequent cracking of underlying structures in the die. Fig. 62 illustrates the results of electrothermal migration. The image shows the positive node of a bump in which voiding at the top edge of the bump has occurred due to the constant bombardment of electrons on that side. In this case, the Pb has migrated to the bottom edge under the influence of the electric field. Figures 62 through 66 show various other common failure mechanisms associated with flip chips.

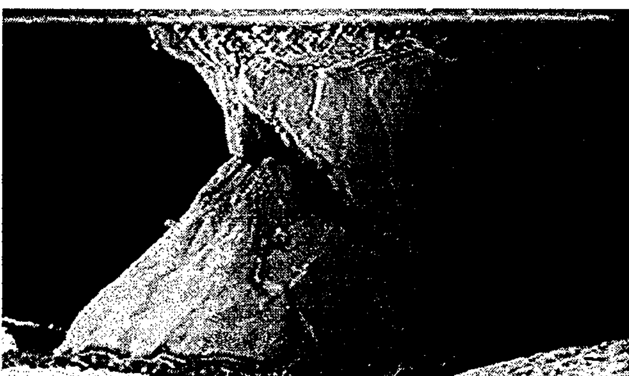

Fig. 60. Example of bump solder creep showing the two interfaces within the device separating from one another.

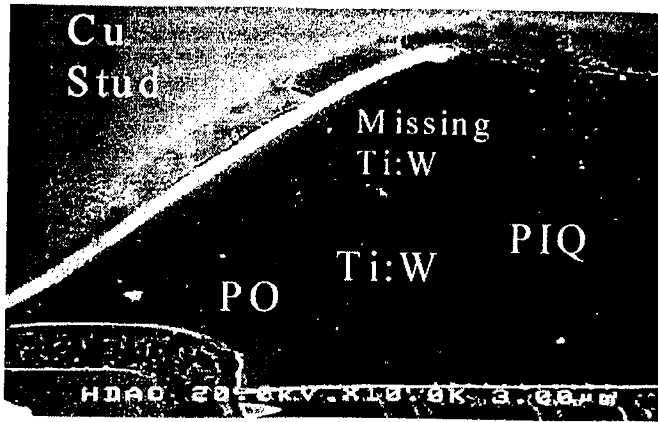

Fig. 61. Image shows lack of Ti:W metal near the cracked area which should extend out through it.

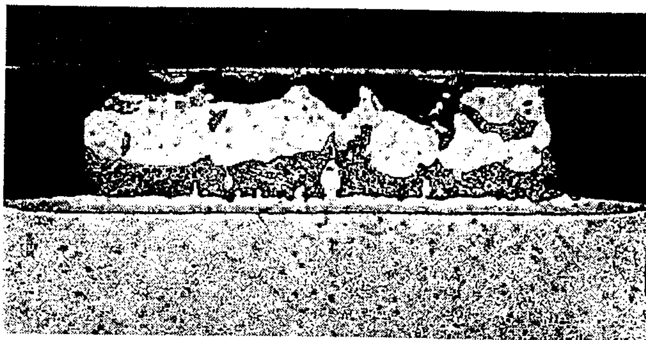

Fig. 62. Effects of the high electric field on the metallurgy within the bump. The image shows the positive node of a bump exhibiting signs of electro-thermal migration.

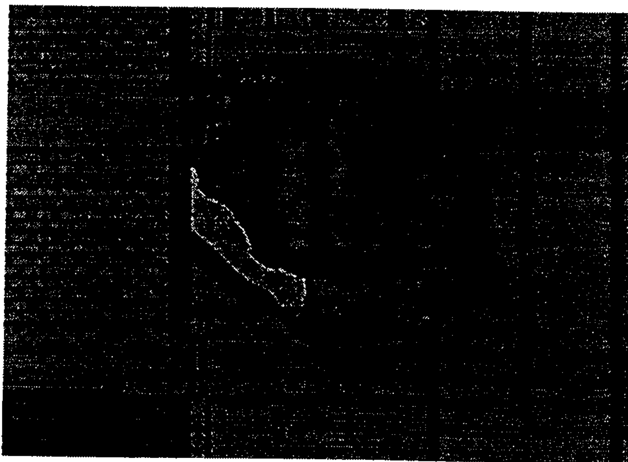

Fig. 63. Image showing a bond pad missing due to an oxide fracture. The fracture is caused by the thermal mismatch of the package to the die.

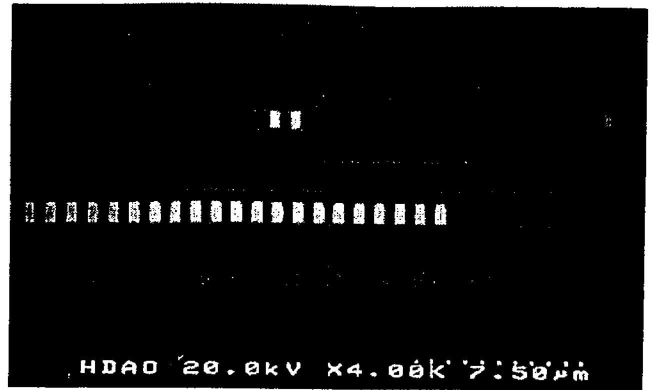

Fig. 64. ILO cracking due to thermo-mechanical package stress at the bump.

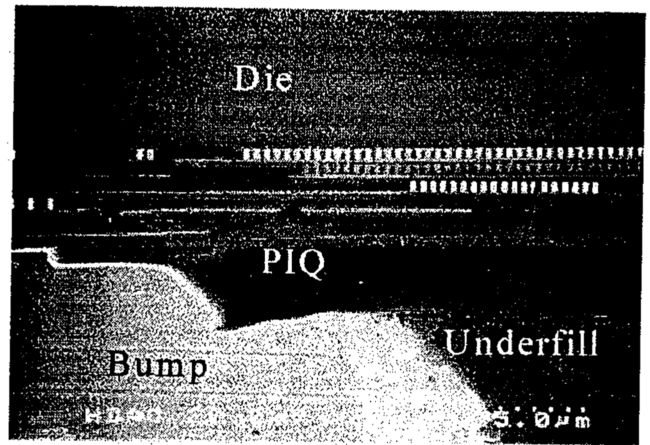

Fig. 65. SEM cross section image of underfill to PIQ delamination due to thermo-mechanical package stress.

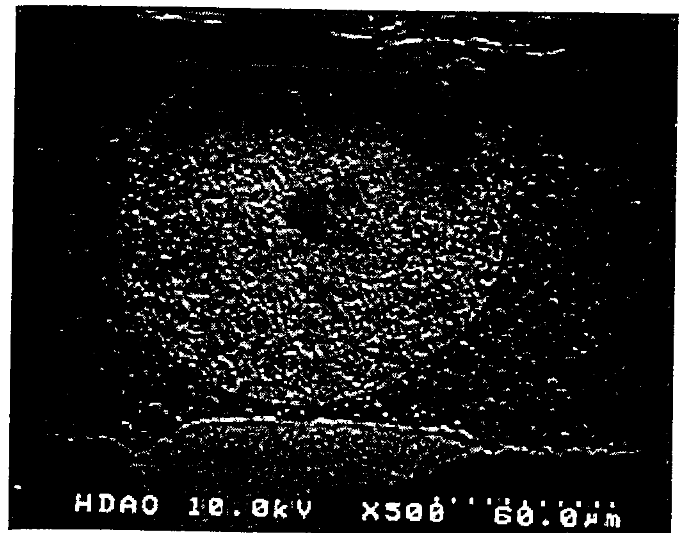

Fig. 66. Image showing a small bump due to the lack of solder plate.

CONCLUSIONS

The journey of the failure analyst is becoming ever more difficult due to the subtlety of the failure mechanisms present in today's devices. It is becoming increasingly important to have an detailed understanding of what the failure mechanism might be before actually finding it. The shrinking geometries of devices have made failure mechanisms out of subtle anomalies that were once irrelevant to the performance of the device. An increased knowledge of device properties on the micro scale has become necessary in order to identify these current failure mechanisms.

The evolution of device architectures has also created new failure mechanisms. One can trace the lineage of failure mechanism back to the most primitive devices. The evolution of the trench capacitor, the multi-level system, and the high aspect ratio contact are all technological advances which tested the abilities of the failure analyst and presented new suspects into the ever increasing file of integrated circuit failure mechanisms. Today, with the growing number of subtle defects which are virtually non- visual, the tools and techniques of the failure analyst are once again put to the test.

Packaging defects have also evolved over time. The mundane packaging issues of the past have given way to more complex issues such as filler damage. Today's packages involve a variety of different materials and some of the greatest problems have occurred due to mismatches in the expansion coefficients within the materials. Today, with the increase in usage of the Flip Chip packaging technology, an extensive knowledge of packaging defects is mandatory.

Inevitably, the list of failure mechanisms will see the addition of new mechanisms as package and device technologies continue to evolve. Thus, the failure analyst must constantly improve the tools and techniques to be able to succeed in the goal of producing needed information and solutions.

ACKNOWLEDGMENTS

The authors would like to acknowledge the entire HDAO Staff for their contributions to this paper. We would also like to thank David Lam and Wilson Tan of TI-Phillipines for images and technical information within the paper. S. Yeh and M. Varnau of Delco are also acknowledged for their images in the flip chip section of the paper.

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